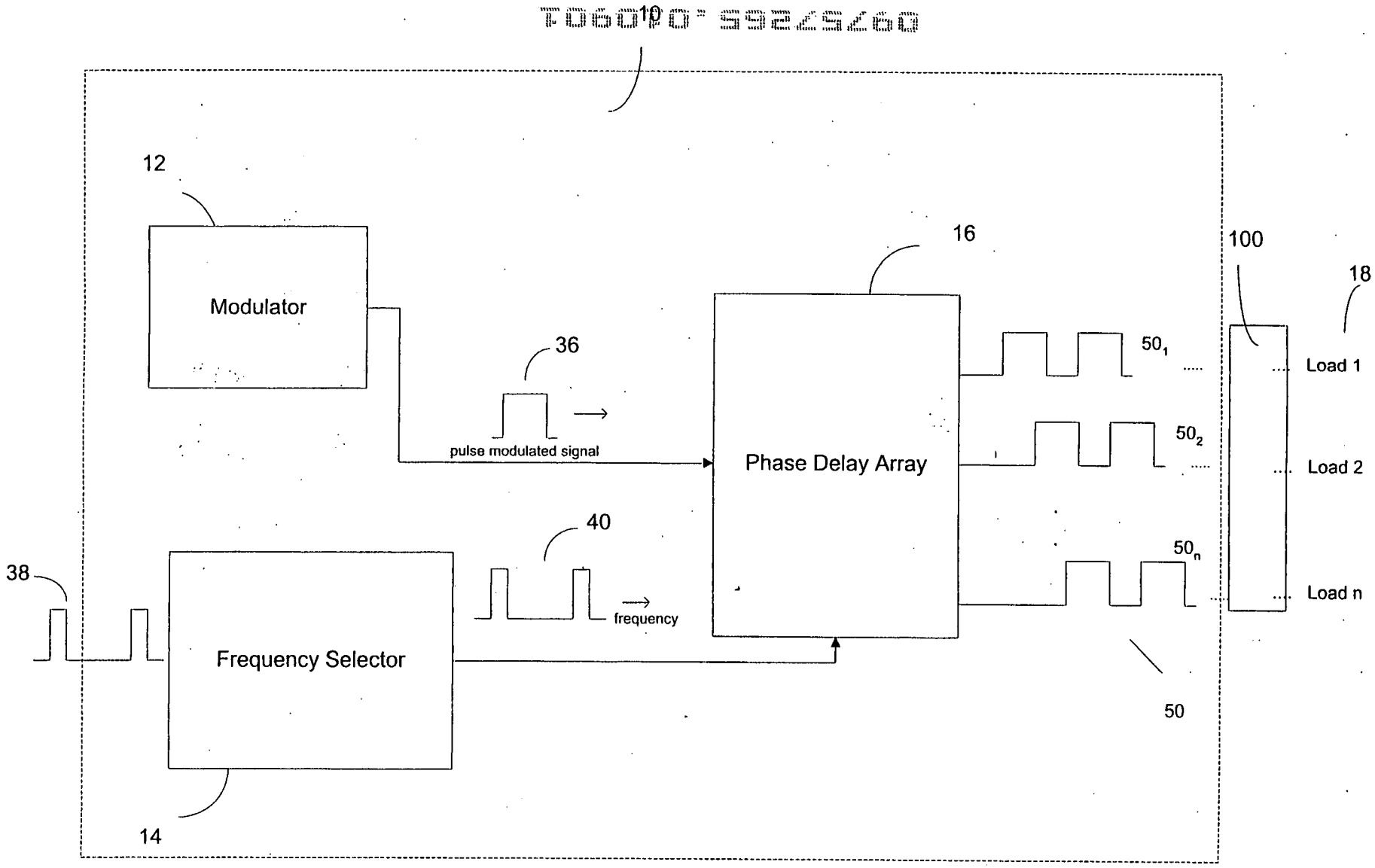

10
12
Modulator
36
pulse modulated signal
16
Phase Delay Array
$50_1$
$50_2$
$50_n$
50
100
18
Load 1
Load 2
Load n
38
40
frequency
Frequency Selector
14

FIGURE 1

TO60TO: 99252260

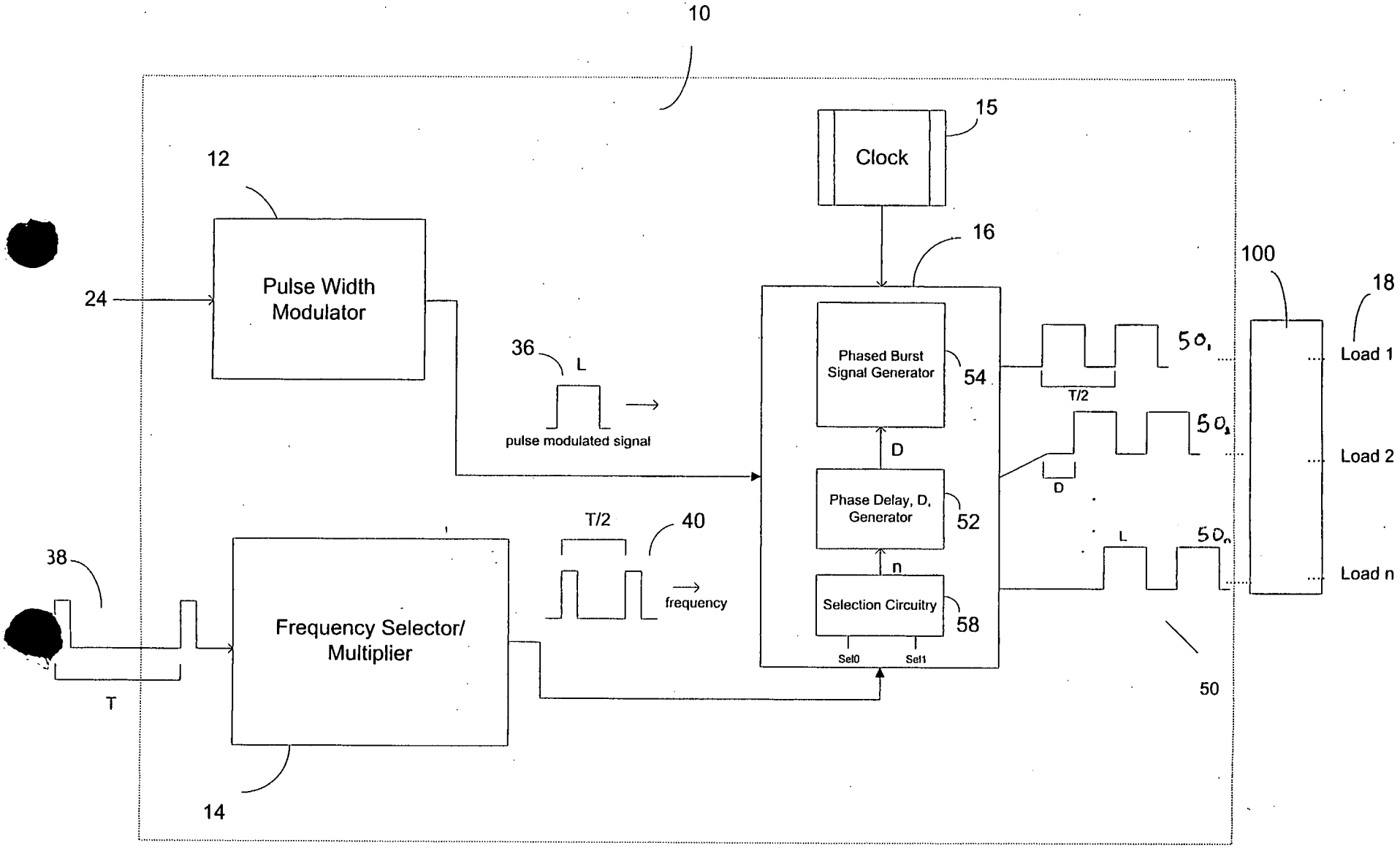



FIGURE 2

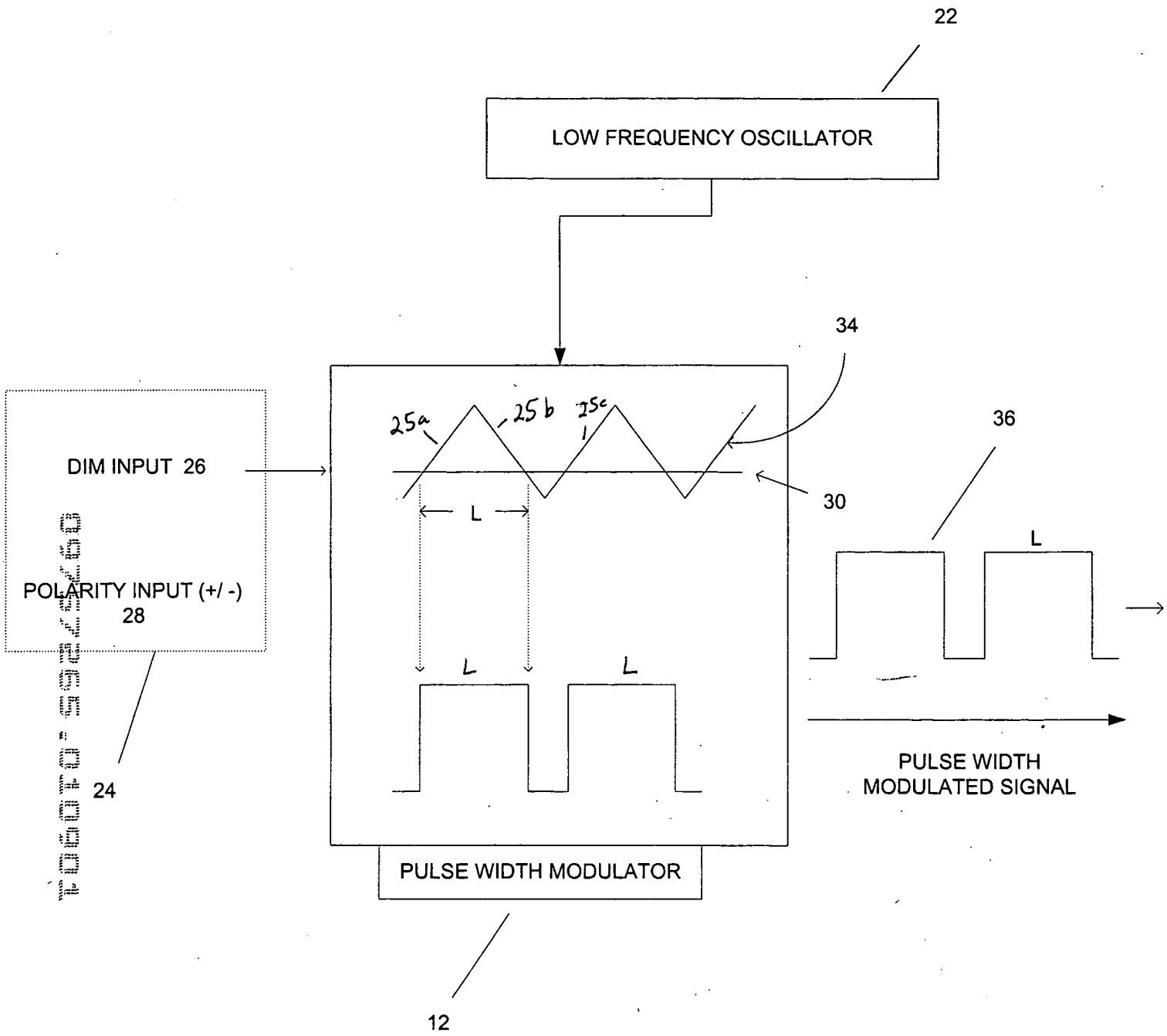

22
LOW FREQUENCY OSCILLATOR
34
25a
25b
25c
36
DIM INPUT 26
30
L
POLARITY INPUT (+/ -)
28
L
L
L
24
PULSE WIDTH
MODULATED SIGNAL
PULSE WIDTH MODULATOR
12

FIGURE 3

Best Available Copy

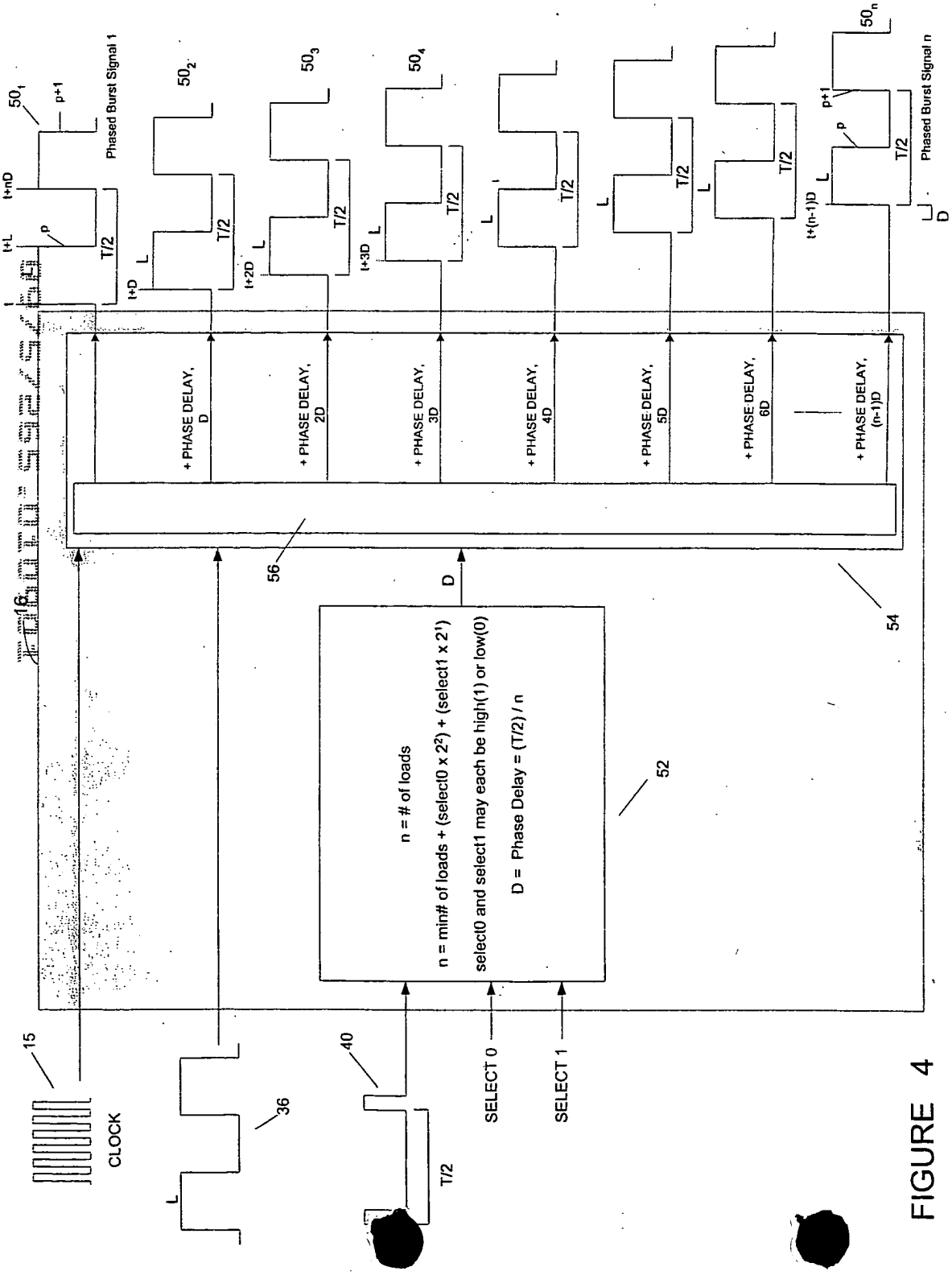



FIGURE 4

| | | | | |
|---|---|---|---|---|
| Sel0 (Select 0) | 0 | 0 | 1 | 1 |
| Sel1 (Select 1) | 0 | 1 | 0 | 1 |
| n (# of CCFLs) | 6 (or min #) | 8 (min # + 2) | 10 (min# + $2^2$) | 12 (min#+2+$2^2$) |

FIGURE 5 (a)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Sel0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Sel1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Sel2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| n (# of loads) | min + 0 | min + 2 | min + 4 | min + 6 | min + 8 | min + 10 | min + 12 | min + 14 |

FIGURE 5 (b)

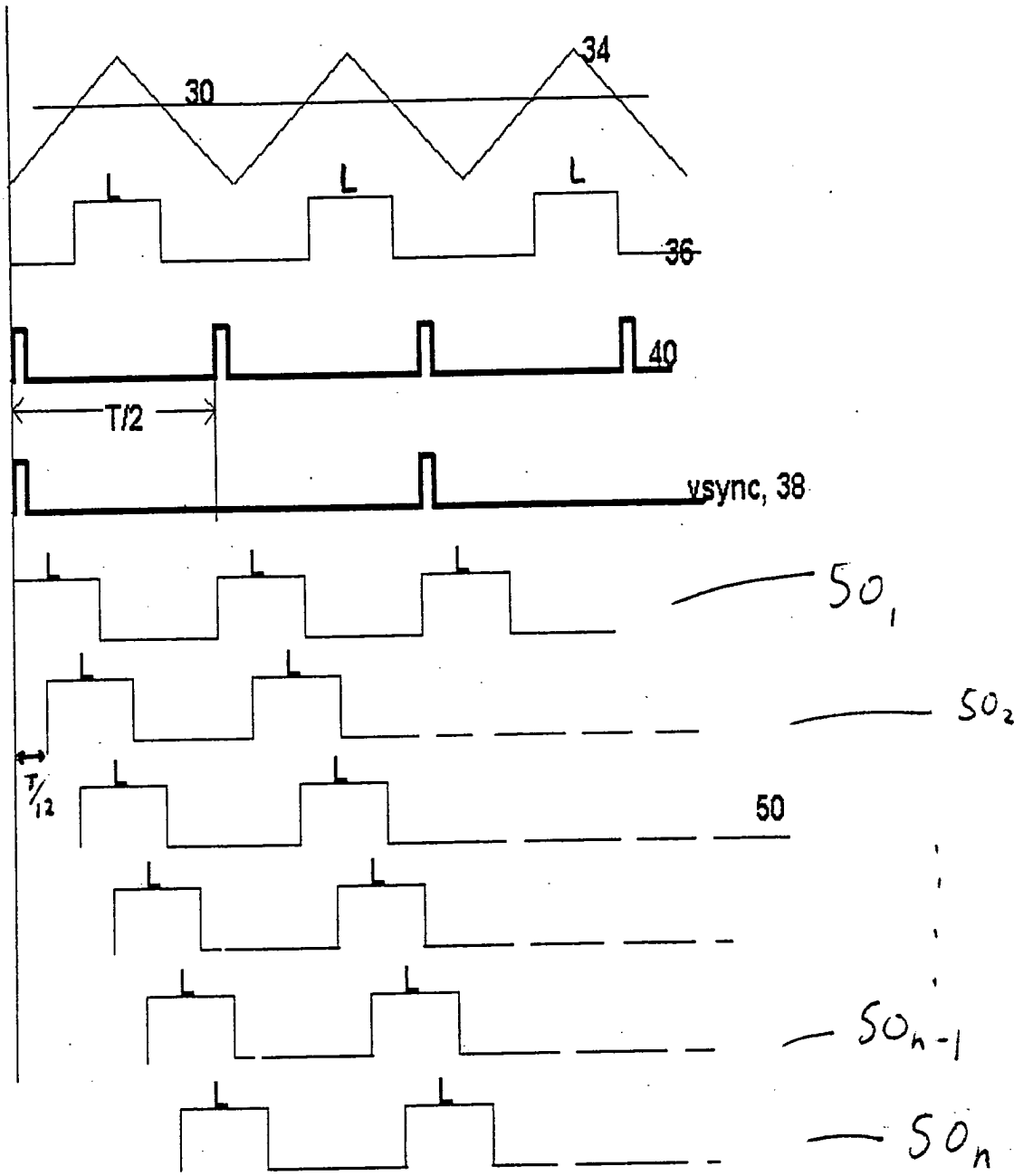



FIGURE 6

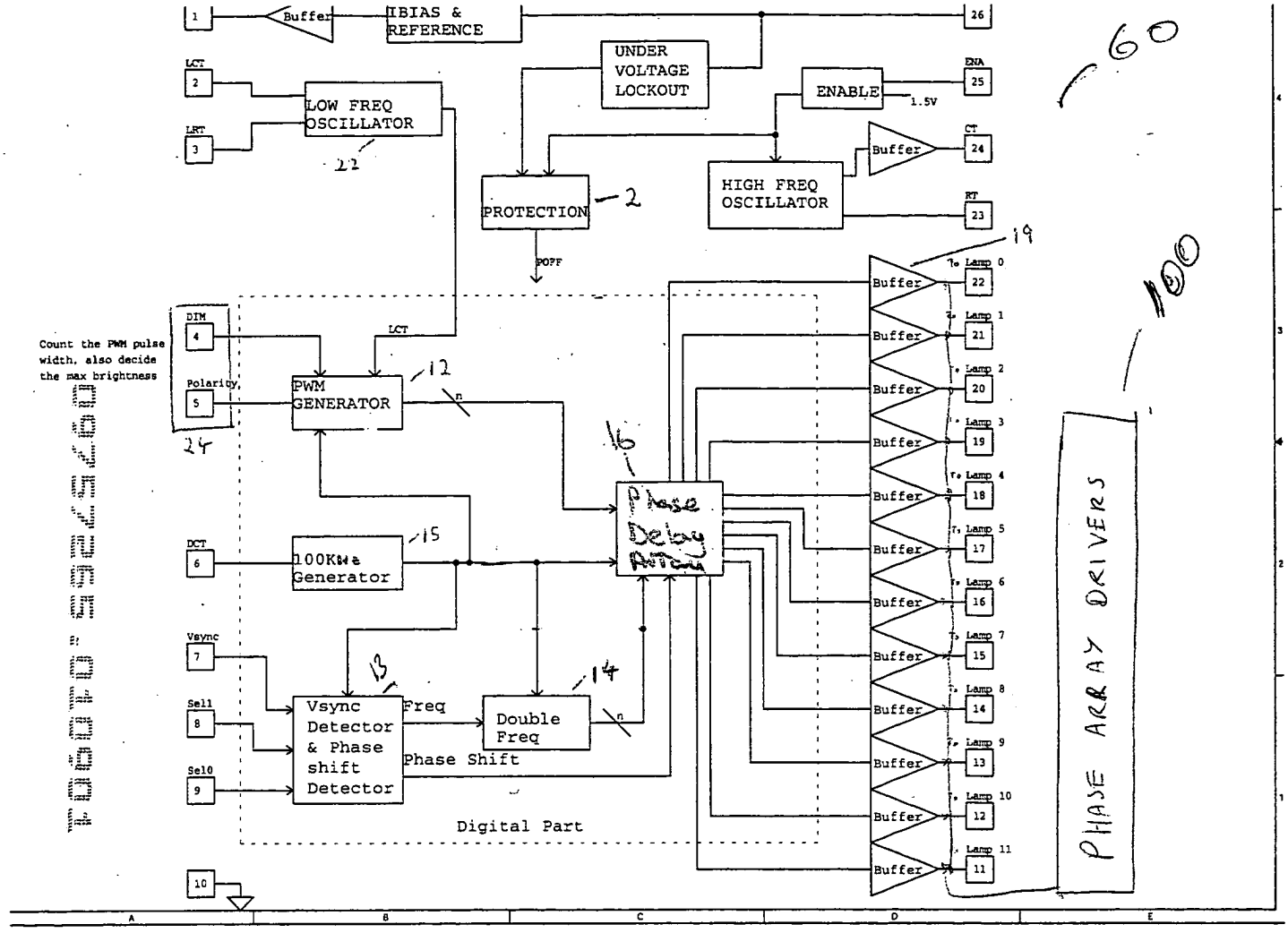

1
Buffer
IBIAS & REFERENCE
26
UNDER VOLTAGE LOCKOUT
LCT
2
LOW FREQ OSCILLATOR
22
LRT
3
ENABLE
1.5V
ENA
25
CT
24
Buffer
HIGH FREQ OSCILLATOR
PROTECTION
2
RT
23
POFF
19
160
100
Count the PWM pulse width, also decide the max brightness
DIM
4
Polarity
5
24
LCT
PWM GENERATOR
12
n
16
Phase Delay Adjust
DCT
6
100K Hz Generator
15
Vsync
7
Sel1
8
Sel0
9
13
Vsync Detector & Phase shift Detector
Freq
Phase Shift
Double Freq
14
n
Digital Part
10
Buffer
Lamp 0
22
Lamp 1
21
Lamp 2
20
Lamp 3
19
Lamp 4
18
Lamp 5
17
Lamp 6
16
Lamp 7
15
Lamp 8
14
Lamp 9
13
Lamp 10
12
Lamp 11
11
PHASE ARRAY DRIVERS
A
B
C
D
E

FIGURE 7

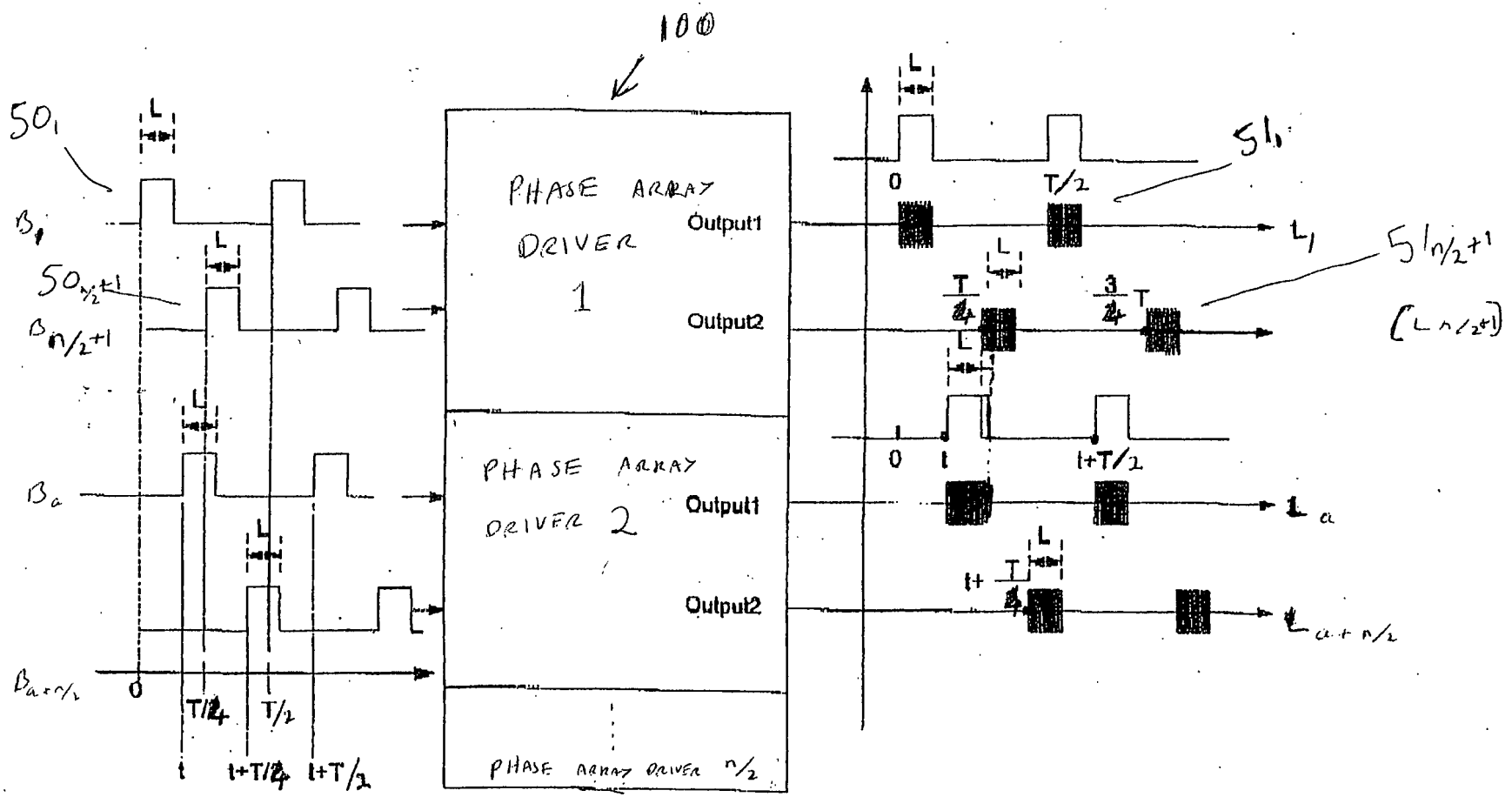

100
PHASE ARRAY DRIVER 1
Output1
Output2
PHASE ARRAY DRIVER 2
Output1
Output2
PHASE ARRAY DRIVER n/2
L
T/2
T/4
3/4 T
t
t+T/4
t+T/2
0

FIGURE 8

TD6070-S92S260

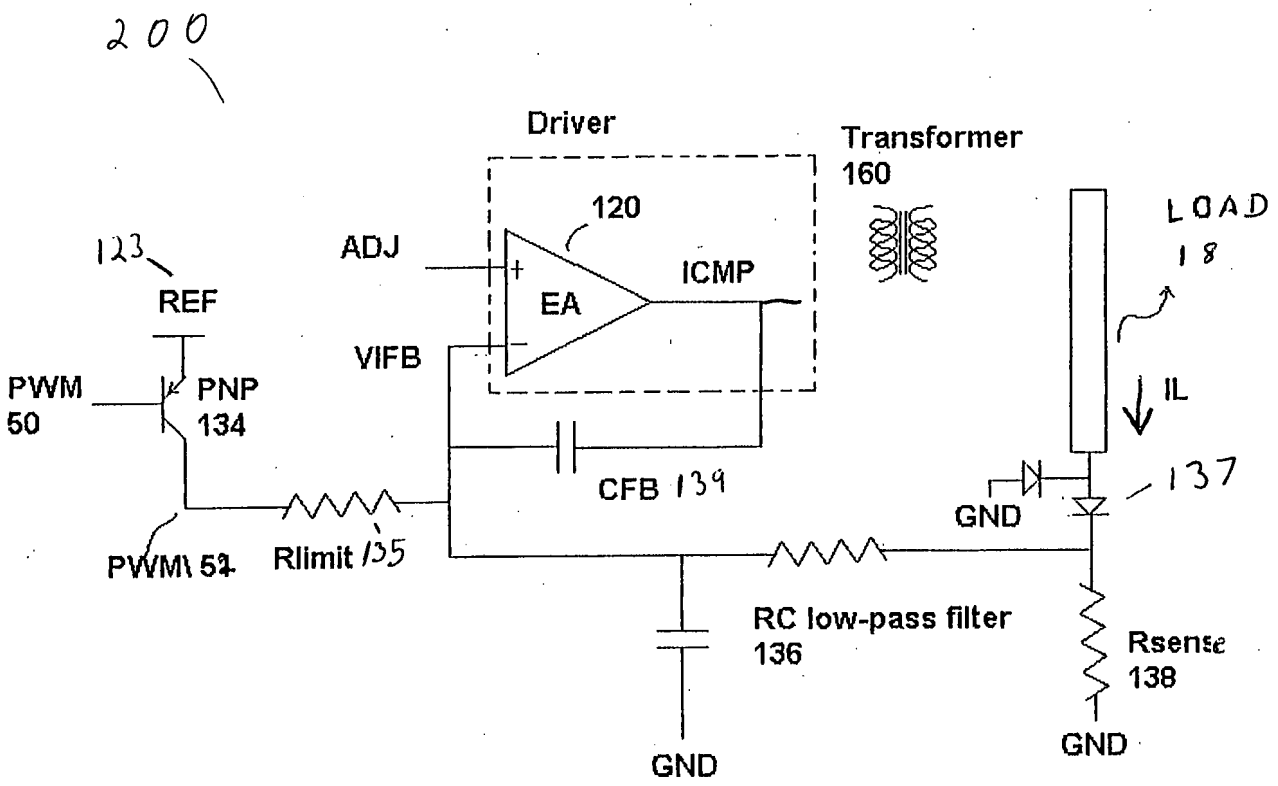



FIGURE 9

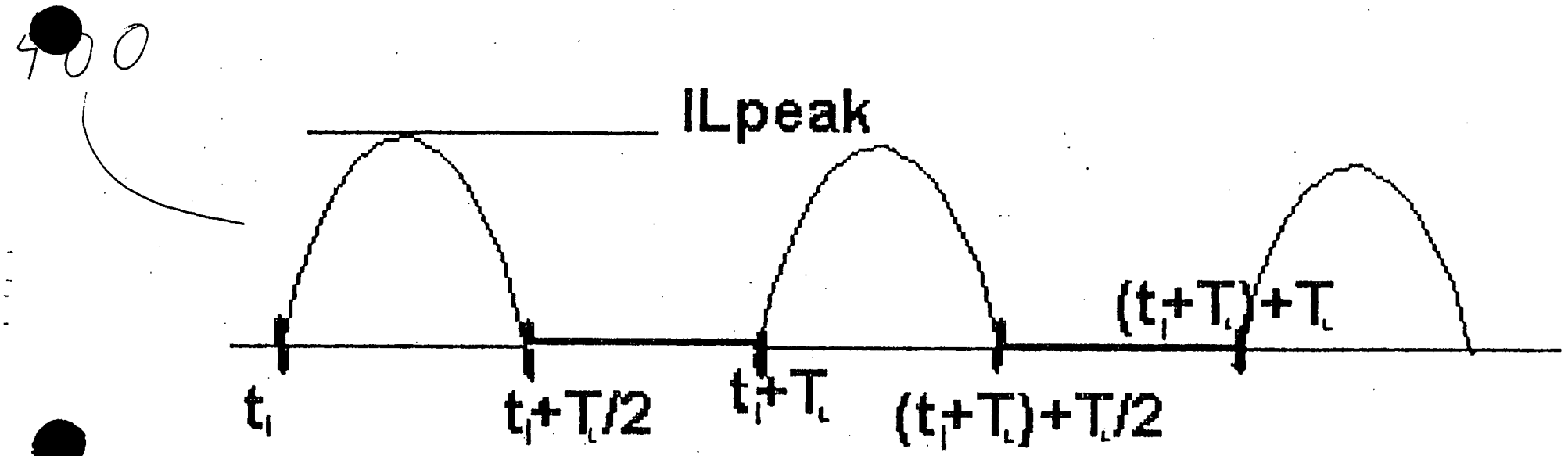



FIGURE 9a

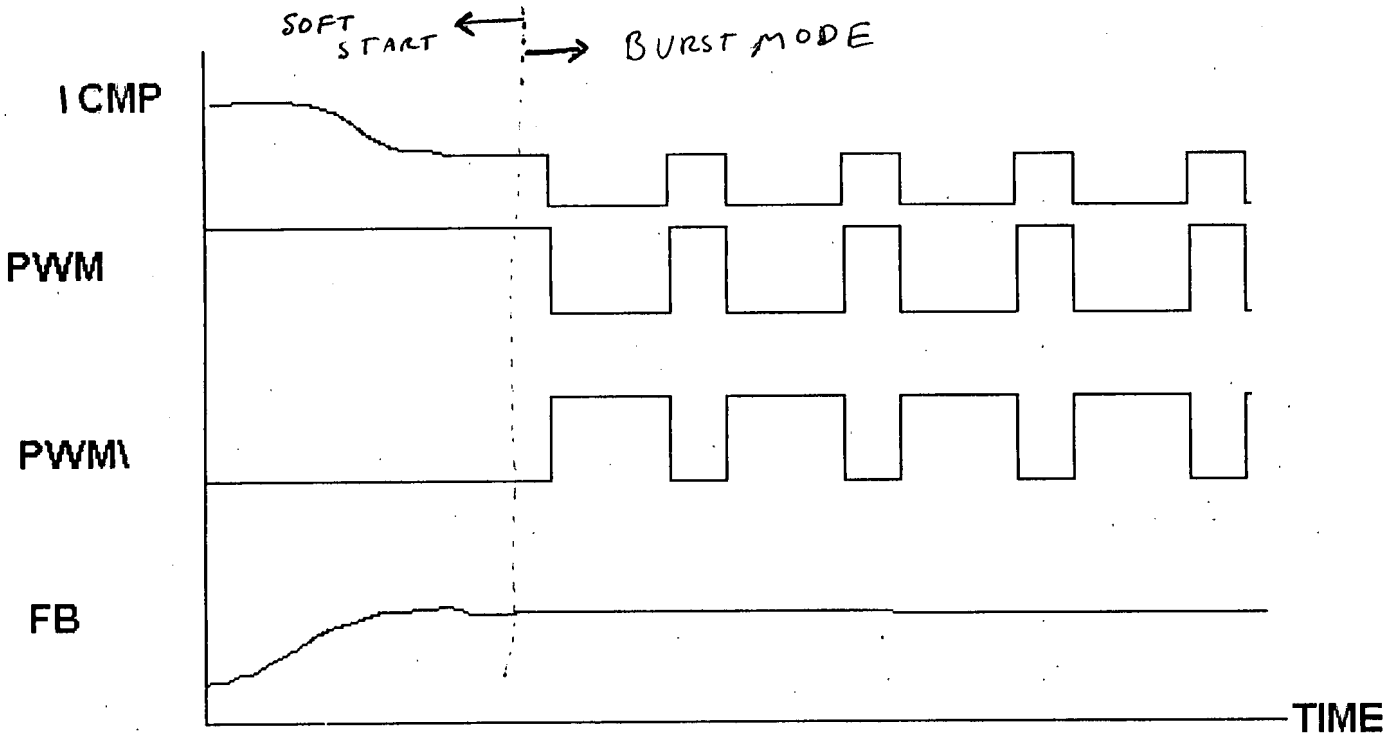



FIGURE 10

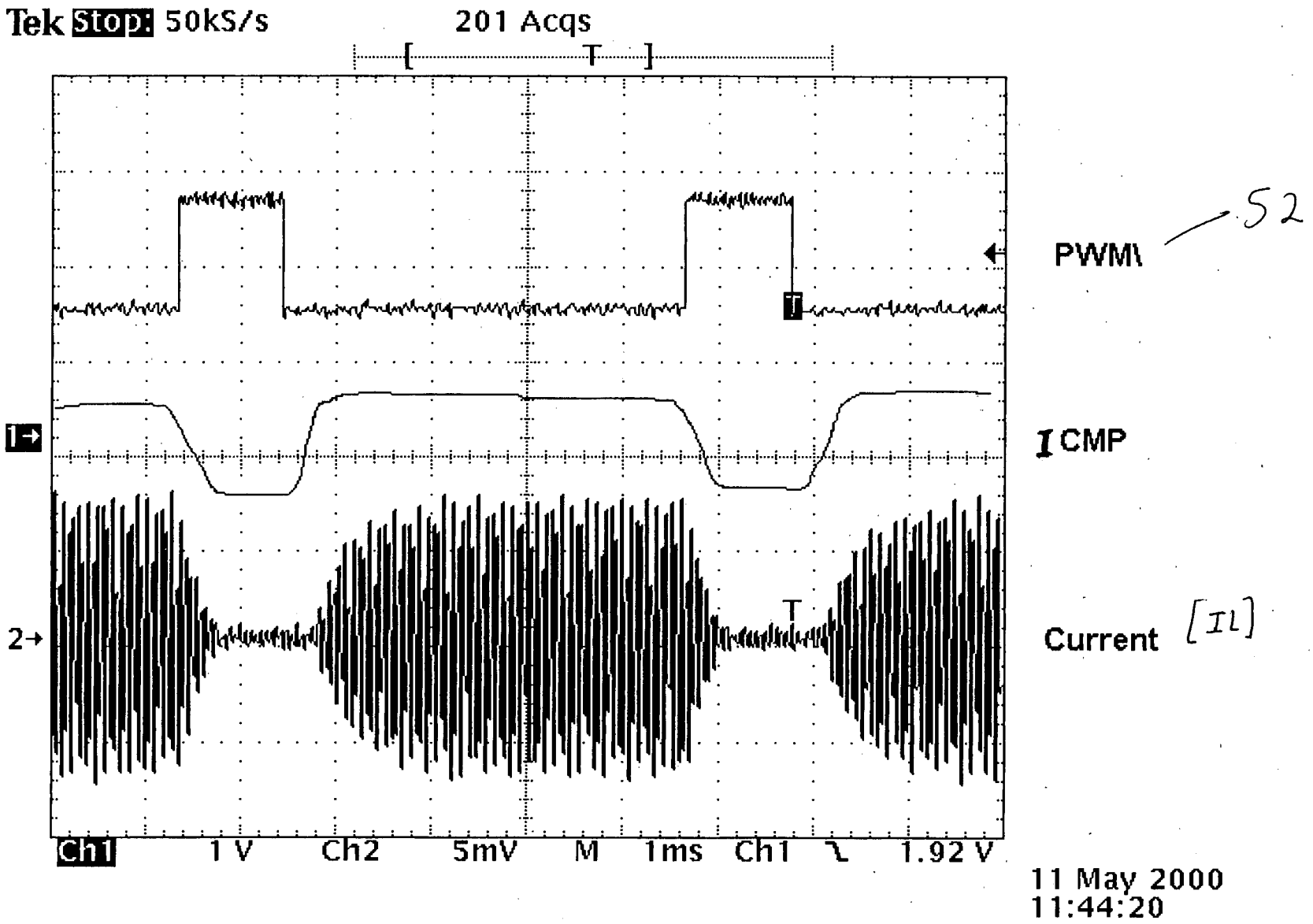

Tek Stop: 50kS/s
201 Acqs
PWM\
52
I CMP
Current [IL]
Ch1 1 V Ch2 5mV M 1ms Ch1 1.92 V
11 May 2000
11:44:20

FIGURE 11

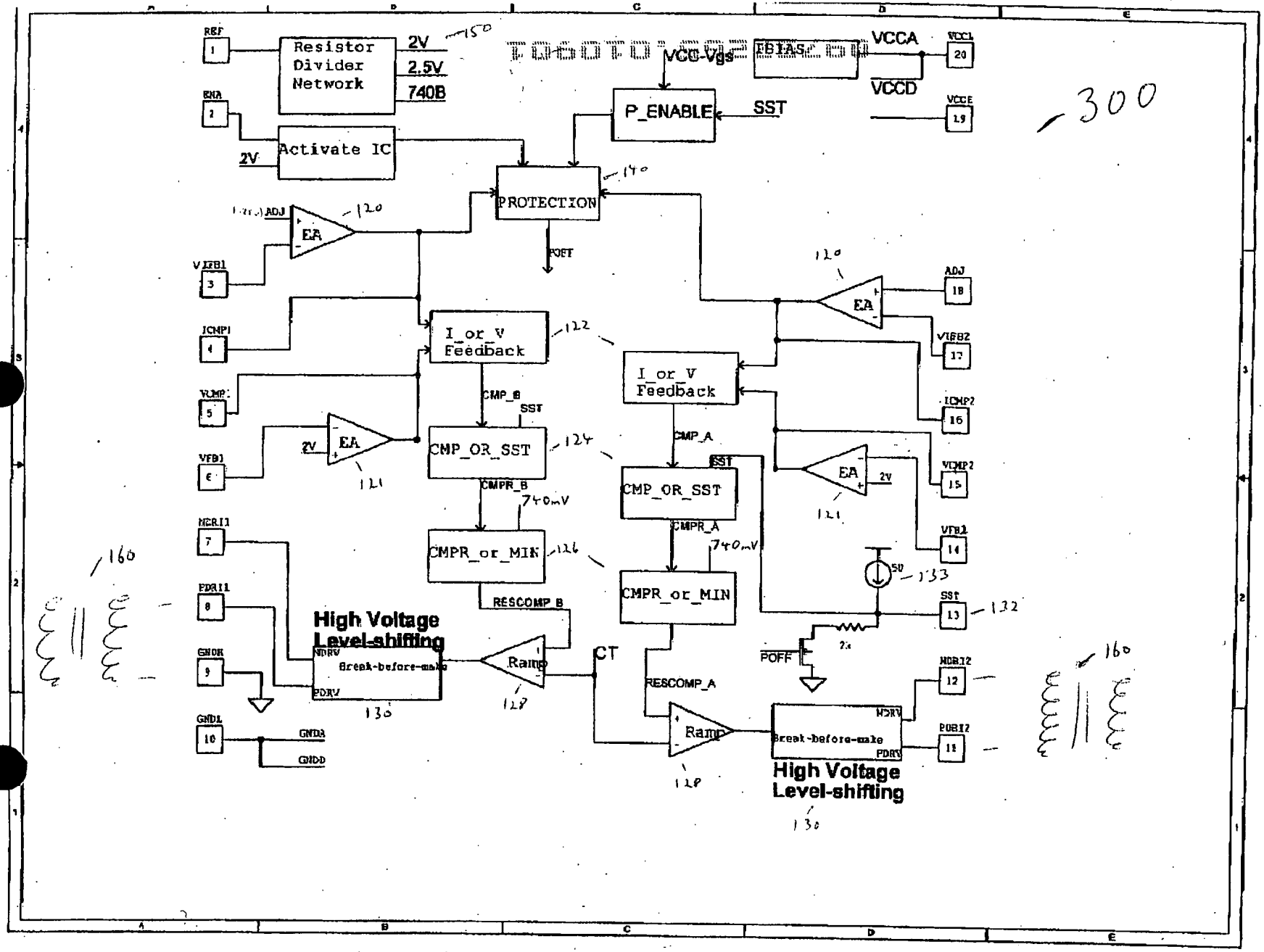

REF
Resistor Divider Network
2V
2.5V
740B
150
ENA
Activate IC
2V
VCC-Vgs
BIAS
VCCA
VCCD
VCC1
20
VCCE
19
P_ENABLE
SST
300
PROTECTION
140
EA
120
ADJ
VFB1
3
POFF
I_or_V Feedback
122
ICMP1
4
VCMP1
5
CMP_B
SST
EA
2V
121
CMP_OR_SST
124
VFB1
6
CMPR_B
740mV
NDRI1
7
CMPR_or_MIN
126
PDRI1
8
RESCOMP_B
GNDR
9
High Voltage Level-shifting
NDRV
Break-before-make
PDRV
130
Ramp
128
CT
GNDL
10
GNDA
GNDD
160
ADJ
18
VFB2
17
ICMP2
16
VCMP2
15
VFB2
14
I_or_V Feedback
CMP_A
SST
CMP_OR_SST
CMPR_A
740mV
CMPR_or_MIN
RESCOMP_A
50
133
SST
13
132
2x
POFF
NDRI2
12
PDRI2
11
High Voltage Level-shifting

FIGURE 12

TO6070 S92S260

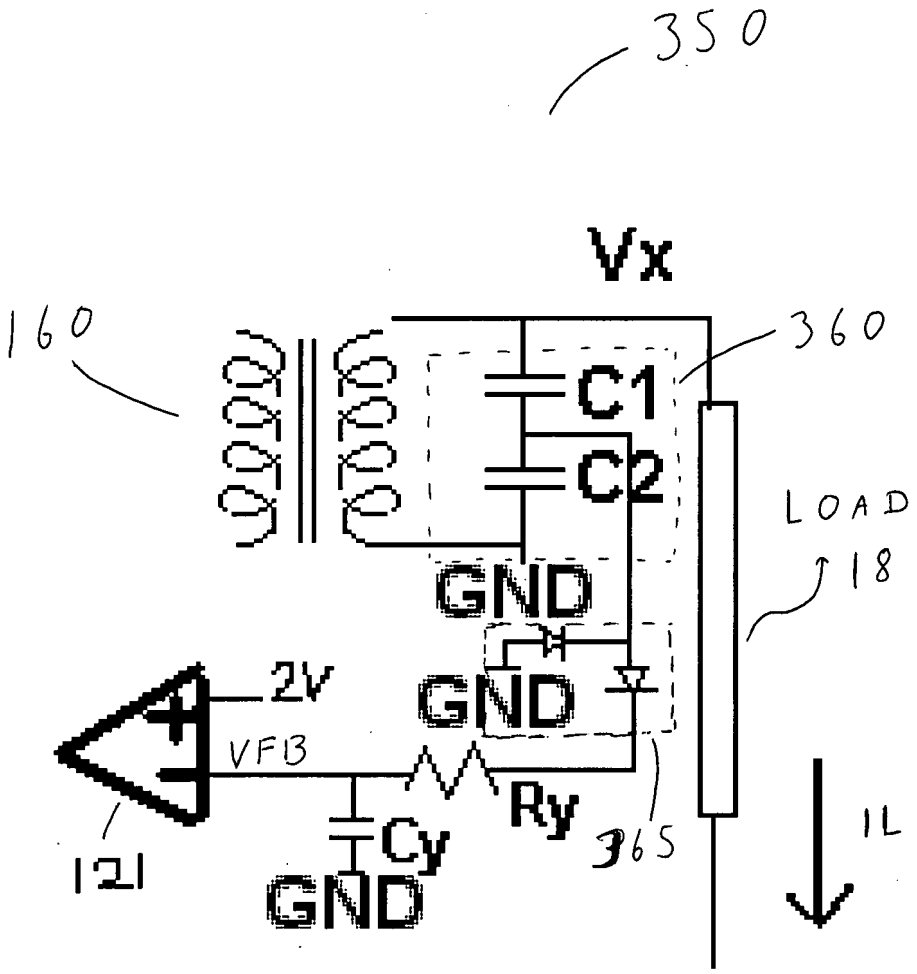
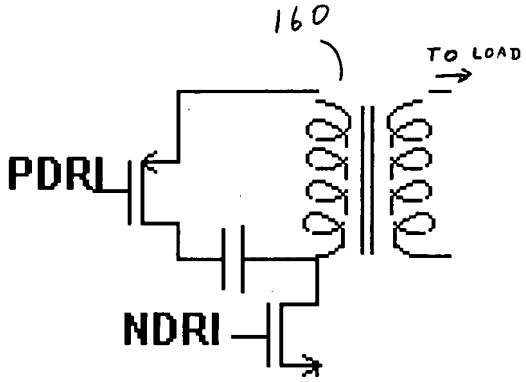
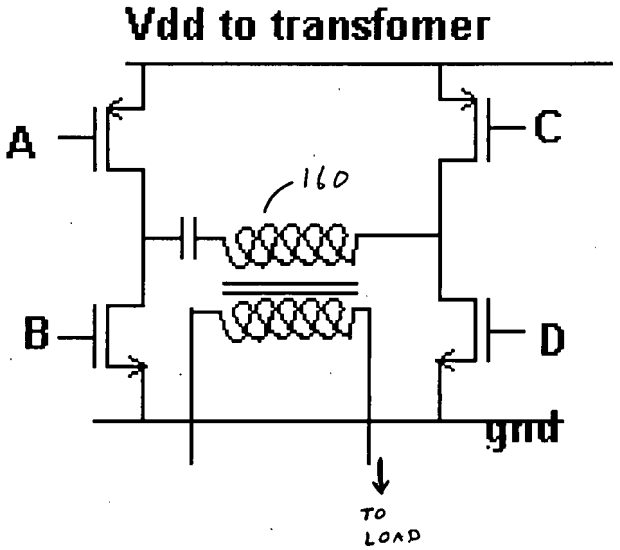



FIGURE 13




14(a)




14(b)

FIGURE 14

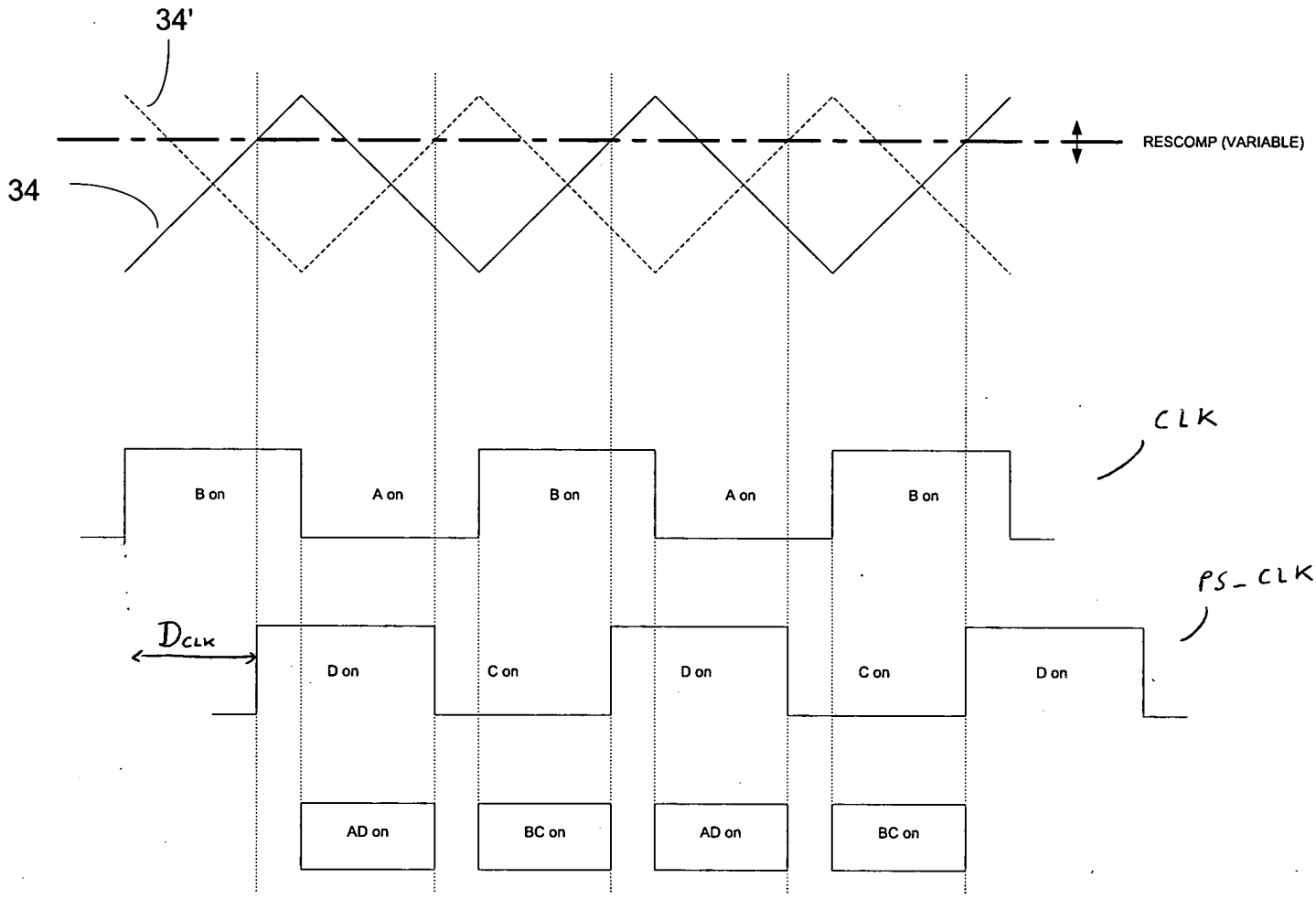

34'
34
RESCOMP (VARIABLE)
CLK
B on
A on
B on
A on
B on
PS_CLK
$D_{CLK}$
D on
C on
D on
C on
D on
AD on
BC on
AD on
BC on

FIGURE 15